

AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): A low capacitance depletion mode SCR and NFET element integrated circuit semiconductor device structure with associated parasitic bipolar transistors on a substrate for the purpose of providing electrostatic voltage discharge protection to the active semiconductor devices, comprising:

[[A]] a first doped region of opposite dopant than said substrate;
a second doped region, of opposite dopant than said first doped region, within said first doped region;
a plurality of third doped regions within said substrate of opposite dopant than said substrate;
a gate element overlaying said substrate surface between a first element and second element of said third doped regions;
a gate element overlaying said substrate surface between a third element and fourth element of said third doped regions;
a first isolation element, in contact with said first doped region, between said second element of said third doped region and a first side of said second doped region;
a second isolation element, in contact with said first doped region, between said third element of said third doped region and a second side of said second doped region;
a plurality of fourth doped regions within said substrate of similar dopant as said substrate;

an electrical conductor system for said second doped region;
an electrical conductor system for said first and fourth elements of said third doped regions
and for the first and second elements of said fourth doped regions; and
a surface passivation layer for said ESD protection device.

Claim 2 (original): The structure according to claim 1 wherein said substrate consists of silicon semiconductor material doped to a concentration between 1E15 and 1E16 a/cm³.

Claim 3 (original): The structure according to claim 1 wherein said first doped region is doped with a donor element such as As to a concentration between 5E15 to 1E18 a/cm³ and has a width between 0.5 to 6 μm and a depth between 0.5 to 6 μm to form a N-well.

Claim 4 (previously amended): The structure according to claim 1 wherein said second doped region is doped with an acceptor element such as boron to a concentration between 1E19 and 1E21 a/cm³ to form a P+ contact region.

Claim 5 (previously presented): The structure according to claim 1 wherein said plurality of third doped regions are doped with an donor element such as arsenic to a concentration of between 1E19 and 1E21 a/cm³.

Claim 6 (previously presented): The structure according to claim 1 wherein said first and fourth elements of the said third doped regions form the N+ source regions of NFET elements.

Claim 7 (original): The structure according to claim 1 wherein said second and third elements of the said third doped regions form the drain regions of NFET elements and are electrically floating.

Claim 8 (original): The structure according to claim 1 wherein said gate elements are comprised of gate oxide to a thickness between 50 and 300Å and polysilicon to a thickness between 3000 and 6000Å.

Claim 9 (previously presented): The structure according to claim 48 wherein said polysilicon is doped with a donor element to a concentration between 1E19 and 1E21 a/cm³.

Claim 10 (original): The structure according to claim 1 wherein said isolation elements consist of shallow trench isolation structures with a width of between 0.1 and 3 µm and a depth of between 0.5 and 4µm.

Claim 11 (original): The structure according to claim 1 wherein said isolation elements are filled with a first layer of SiO₂ to a thickness of between 50 and 500 Å and then filled with a second layer of SiO₂ to said substrate surface.

Claim 12 (previously presented): The structure according to claim 1 wherein said plurality of fourth doped regions are doped with an acceptor element such as boron to a concentration of between 1E19 and 1E21 a/cm³ to form P+ contact regions for said substrate.

Claim 13 (previously presented): The structure according to claim 1 wherein said electrical conductor system for said second doped region consists of aluminum metallurgy or aluminum doped with 1% silicon metallurgy, and is connected to a first voltage source consisting of the input pad of said active semiconductor devices.

Claim 14 (previously presented): The structure according to claim 1 wherein said electrical conductor system for said first and fourth elements of said third doped regions consists of aluminum metallurgy or aluminum doped with 1% silicon metallurgy, and is connected to a first voltage source consisting of the input pad of said active semiconductor devices.

Claim 15 (original): The structure according to claim 1 wherein said surface passivation layer for said ESD protection device consists of deposited SiO₂ doped with boron and phosphorous to form BPSG.

Claims 16 – 37 (previously canceled)

Claim 38 (new): The structure according to claim 1 wherein said first and second isolation elements are in contact with said substrate.